R E M A R K S

Reconsideration of the above-identified patent application is respectfully requested in view of the foregoing amendments and the following remarks. Claims 1 - 8 were previously canceled. Claims 11 - 14 are withdrawn. Claims 9 and 10 have been amended and remain in the case.

Applicants acknowledge that the claim for priority under 35 U.S.C. §120 has not been properly incorporated in the application. The specification has been appropriately amended.

The drawings were objected to, specifically because FIGURE 2 required the legend "Prior Art," and FIGURE 4 did not show the "intermetallic boundary interface." The drawings have been amended and new copies have been provided with this response.

While an intermetallic boundary is now shown in FIGURE 4, it can, of course, only be an approximation. As Examiner Garcia is no doubt well aware, the intermetallic boundary

formed during a soldering operation is, at best, difficult to define, describe, or quantify. Not only is this boundary region dependent on the specific materials involved, it also changes over time, never becoming completely stable. For example, if the pad has a gold wash for wetting purposes, the gold rapidly diffuses into the tin-lead solder. The tin and/or lead are much slower in their rates of diffusion. Consequently, the precise extent of the boundary layer is inexact. The intermetallic boundary region shown in FIGURE 4 is a schematic approximation, not an attempt to show to scale the exact extent of the material diffusions or other processes creating an intermetallic region.

The specification was objected to because the language of claim 10 regarding "intermetallic boundary interface" was not properly supported. Claim 10 has been amended and Applicants believe that the recitation of claim 10 is properly supported in the specification. Therefore, the objection has been overcome.

Claims 9 and 10 were rejected under 35 U.S.C. §102(b) as being anticipated by Japanese Patent No. 62-15844 for

SEMICONDUCTOR LEAD FRAME, published January 24, 1987 upon application by Asao Nishamura et al. NISHAMURA et al. teach a structure completely different from that of Applicants' substrate configuration. Refer to FIGURE 2 of NISHAMURA et al., an enlarged reproduction of which was kindly provided to Applicants by Examiner Garcia. A suspended lead 4, presumably metallic, has a tab 1 at a distal end or possibly a central portion thereof and axially aligned therewith. Tab 1 has a corrugated part 2 formed in tab 1 by a press when the lead frame is fabricated. A semiconductor chip 6 having a flat bottom surface is positioned above corrugated part 2. The flat bottom surface of semiconductor chip 6 touches only the uppermost portions of corrugated part 2 leaving a gap 12 between the bottom surface of semiconductor 6 and the top of corrugated part 2. Gap 12 is filled with a bonding material 9 comprising silver paste and solder.

The stated function of the NISHAMURA et al. structure is to compensate for "different thermal expansions among semiconductor-package constituting materials." Applicants assume that this is equivalent to CTE. When bonded to semiconductor chip 6, corrugated portion 12 of tab 1 is

flaccid and free to move, most likely with at least two degrees of freedom, to accommodate any variation in semiconductor chip 6.

After assembly, semiconductor chip 6, suspending lead 4, and tab 1 with corrugated part 2 are all encapsulated in resin 8. Once assembled, the bond formed between semiconductor 6 and tab 1 is probably not subject to contact fatigue due to the propagation of micro-cracks in the intermetallic boundary. In fact, because no details are given in the English language translation of what Applicants assume is the Abstract of Japanese Patent 62-15844, it is not clear what the nature of a developed intermetallic layer, if any, might be.

Applicants' structure, on the other hand, comprises a rigidized pad, affixed to a substrate such as a printed circuit board (PCB) or the like. There is no corrugated, cantilevered lead, but rather an undulating, solid surface. No semiconductor chip is directly affixed to Applicants' surface, leaving a gap in the valleys. The surface is adapted to receive a solder ball or the like. Upon reflow or when otherwise heated, the solder ball flows into the valleys of

Applicants' undulating surface and adheres to the complete surface.

An intermetallic region roughly conforming to the surface topography of the pad is formed where there is a metallurgical bonding of the materials of the solder and the pad. It is in this thin, intermetallic region that stress-induced micro-cracks have been found to develop. Applicants' undulating or otherwise non-planar pad surface has been found to limit the propagation of such micro-cracks. The substantially flat pad surfaces of the prior art were susceptible to straight line cracking, generally propagating across the complete solder joint. Unlike that of NISHAMURA et al., Applicants' structure is not designed to compensate for differences of CTE but to interrupt the spread of micro-cracks. Because the functions vary so considerably, each structure is likewise completely different.

Claims 9 and 10 have been amended to more clearly recite a structure deemed to be patentably distinct from the lead frame structure disclosed by NISHAMURA et al. Consequently, Applicants believe that the rejection of claims 9 and 10 under

35 U.S.C. §102(b) has been overcome and respectfully request that the claims be allowed and the application be passed issue.

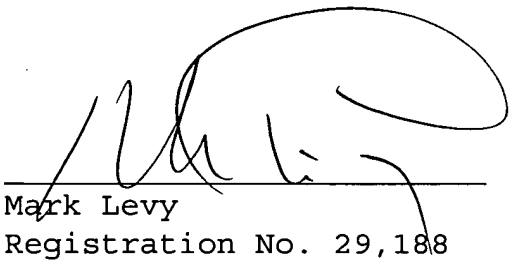
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to:

Mail Stop _____
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

On 9/5/03
(Date of Deposit)

Mark Levy, Reg. No. 29,188 9/5/03
Attorney (Date)

Respectfully submitted,



Mark Levy
Registration No. 29,188
Attorney for Applicants
Press Building - Suite 902
19 Chenango Street
Binghamton, New York 13901

Phone: (607) 722-6600